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## ANOTHER WAY OF DIAGRAMMING SWITCHING CIRCUITS

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The relationship between symbolic logic and switching circuits is susceptible to an interesting treatment if we introduce the use of more complicated switches than the single-pole single throw (SPST) switches commonly found in diagrams. A single-pole double-throw switch (SPDT) can control more complex circuitry, as Figure 1 shows. The SPST can open or close only circuit  $C_1$ , while the SPDT switch can control both circuits  $C_2$  and  $C_3$ , although it cannot close both at the same time, a useful fact. If the SPST switch is used to represent the values of a variable, P, then when the switch is closed, this is used to represent P as true, or as having the value 1, and when the switch is open, this represents P', or P as having the value 0. The SPDT can be used to the same end, but represents P when closed on one side, and P' when closed on the other. Thus, circuit  $C_2$ , when activated, could represent P, and circuit  $C_3$ , when activated, represents P'.

If we employ two variables, P and Q, and one SPDT switch for each, an incomplete circuit such as the one in Figure 2 might be constructed. If to this certain additional connections be added, between the points of the P and Q switches, as would be necessary to make a complete circuit possible, these connections can be so made as to permit completion of the circuit, by throwing of the switches, only if one of the 16 functional relations between P and Q is satisfied. If, for example, we want the circuit closed only if Pand Q have the value 1, which amounts to Conjunction, a connection may be made as in Figure 3. This circuit will be closed only if the switches are set at P and Q.

If the two SPDT switches are given simplified representation as in Figure 4, where the arrows indicate further connection into the circuit, all the useful connections between the points of those switches will be as shown and numbered. Each of the four connections in the figure corresponds to one row in the truth-table for P and Q, numbering the rows as follows:

Row	P	Q	$F_1$
1	1	1	1
2	1	0	0
3	0	1	0
4	0	0	0

The function  $F_1$ , Conjunction, is established in the circuitry by the use of connection 1 in Figure 4, corresponding to Row 1 of the truth-table. A function such as Material Implication, which would have the values 1011 in a truth-table column, i.e., 0 only in Row 2, could be set up in the circuitry by the omission only of connection 2 in Figure 4. Figure 5 shows some of the more important functions of P and Q using this system. Tautology will be represented by the presence of all connections, just as in Figure 4, while Contradiction would involve the absence of all connections, so that the circuit cannot be completed. Circuitry for all the other functions can easily be found.

An interesting property of this system is that logical operations can be performed using only the diagrams. Alternation, for example, is additive in the diagrams, so that  $[(P \& Q) \lor (P' \& Q')]$ , Material Equivalence, merely adds the connections for Conjunction to those for Neither-Nor, as can be seen in Figure 5. The operation of Conjunction can be performed by a process of subtraction: to conjoin the functions represented in the diagrams, one subtracts (rejects) all those connections that they do not have in common. Thus, the conjunction  $[(P \lor Q) \& (P \supset Q)]$  would involve only those connections common to both Alternation and Material Implication, as shown in Figure 6. This is confirmed in a truth-table, where  $[(P \lor Q) \& (P \supset Q)]$  has the values 1010 in its column, so that just as Rows 1 and 3 in the table have the value 1, only connections numbered 1 and 3 in the diagrams remain.

The operation of Negation is complementary in these diagrams. The formula  $(P \supset Q)'$ , for example, involves in its diagram only those connections that do not exist for Material Implication, as shown in Figure 7. Again, this may be compared with a truth-table.

Any function of P, of Q, or of both, can be represented diagrammatically after reference to their truth-tables. For example, P, as well as  $P \& (P \lor Q)$ , have the truth-table column 1100, for which the circuit is shown in Figure 8. Taking advantage of the operations possible with these diagrams, we can even find equivalent formulae, e.g., we can generate the circuit in Figure 8 by the process shown in Figure 9. This corresponds to  $[(Q \supset P) \& (P \lor Q)] \equiv [P \& (P \lor Q)]$ . It can also be seen that the circuit in Figure 8 is equivalent to  $[(P \& Q) \lor (P \& Q')]$ , i.e., the alternation of the values of P and Q in Rows 1 and 2 of their truth-table, which corresponds to the addition of connections 1 and 2.

The extension of the system to three variables calls for the introduction of yet another type of switch, the double-pole double-throw (DPDT). Where P, Q, and R are the three variables, P can still be represented by a SPDT switch, but Q and R will be represented by DPDT switches. Such a switch connects parts of a circuit to either of two pairs of points, and thus operates like two SPDT switches tied together. Figure 10 shows how the SPDT switch for P and the two DPDT switches for Q and R would actually be connected. Fortunately, we can transform this into the diagram of Figure 11. At point X, one pole of the DPDT switch for Q is connected to the 'true' point of the switch for P, and at point Y a connection is made between the other pole of the Q switch and the 'false' point of the P switch. Thus, as indicated, one branch of the circuitry will function under P, and the other under P'.

Each numbered connection in Figure 11 corresponds to one row in the truth-table for the three variables, numbered as follows:

Row	Ρ	Q	R	$F_1$
1	1	1	1	1
2	1	1	0	0
3	1	0	1	0
4	1	0	0	0
5	0	1	1	0
6	0	1	0	0
7	0	0	1	0
8	0	0	0	0

 $F_1$ , the conjunction of P, Q, and R, has 0 everywhere but in Row 1, and correspondingly its representation in the diagrams would omit all but connection 1 in Figure 11. For convenience in drawing, the unconnected parts of the switches can be represented by circles or dots, as in Figure 5. All of the functions of three variables can likewise be given a circuitry, following the parallel between their truth-tables and the numbered connections in Figure 11. Operations can be performed using the diagrams, just as before, except that now more figures must be attended to. Where an operation (such as Conjunction) is to be performed on diagrams involving more than one X-like figure, such as diagrams of functions of P, Q, R, each figure must be dealt with in association with the figure having the same position in another diagram. Thus, right-hand figures are dealt with together, left-hand figures together, and so on.

The extension of the system to more than three variables can readily be accomplished, but involves the use of more figures, just as truth-tables become longer, and just as we require more complex switches, e.g., 4PDT. In general, where *n* variables  $(V_1, V_2, V_3, \ldots, V_n)$  are involved, with their truth-table having  $2^n$  rows, then all functional relations can be covered by a system of switches having for  $V_1$  a SPDT switch, for  $V_2$  a DPDT switch, for  $V_3$  a 4PDT switch, etc., but for  $V_{n-1}$  and  $V_n$  each a  $\frac{2^n \text{PDT}}{4}$  switch. Since every switch will have 2m points, where the switch is *m*PDT, and since every point of every switch will have two possible connections into the points of the next switch, following the pattern used above, the  $V_{n-1}$  switch will have  $2^n$  possible connections into the  $V_n$  switch. In that way, all  $2^n$  possibilities can be accounted for.

For any set of variables  $V_1 \ldots V_n$ , only the figures for the switching connections of the last two variables are used in this system of diagrams. If four variables are involved, the last two,  $V_3$  and  $V_4$ , will each require a 4DPT switch, and their connections can be represented in a series of four X-like diagrams. There will be 16 connections represented, accounting for all possible relations between all four variables. For a function of three variables, two X-like figures are required, one functioning under P and one under P', as was noted. Where four such figures are needed, for four variables, one will function under P & Q, one under P & Q', one under P' & Q, and one under P'&Q'. In the performance of operations with the figures, however, all that needs to be attended to is the X-like figures. A certain simplicity is thus attainable, although the number of figures that must be used does, of course, increase as the number of variables increases. An actual "logical machine" could easily be constructed using the system here described, since the diagrams, although simplified, correspond to physically possible circuits. The numbered connections between the points of the switches for the variables could be controlled by a set of SPST switches instead of by connecting or disconnecting wires. The machine could show, e.g., by a lamp, that only certain values of the variables make possible a completed circuit.

The system discussed here can be used not only to set up switching circuits involving any number of variables, but to study and operate with functions themselves. Moreover, it is a mechanical system, requiring no ingenuity. It eliminates the duplication of switches for the same variable in a single diagram, which is often necessary where SPST switches alone are used. Once set up for a certain number of variables, only the most elementary adjustments permit any function to be represented. There is the further advantage that an isomorphism with truth-tables is achieved.

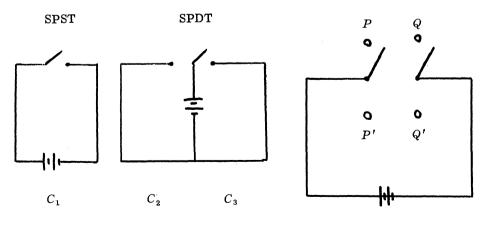
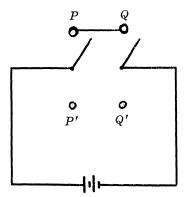
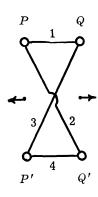


Figure 1

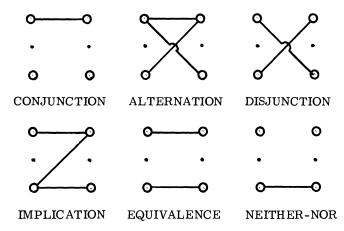
Figure 2













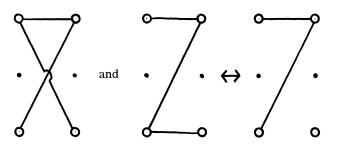
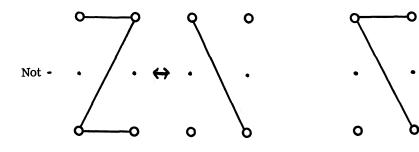


Figure 6







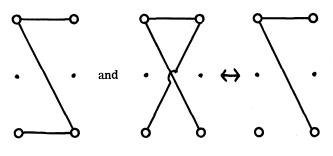


Figure 9

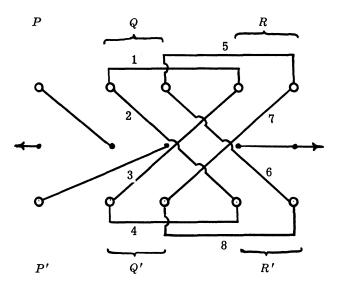


Figure 10

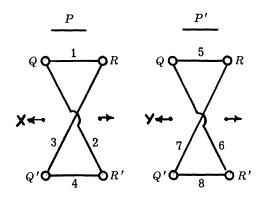


Figure 11

Note added April 9, 1976: Unfortunately, it is necessary to add a prohibition against a certain use of the switches. Where the switching diagrams contain three lines or connections, corresponding to functions with only one "F" or "0" in their truth-tables, the circuit will always, and undesirably, be completed whenever both switches are so set that the switch blades contact points that are singly connected. By "singly connected" I mean a point to which only one wire is connected. Thus, in the diagram for Material Implication, which is shaped like a "Z," if the P switch is set upwards (P is true) and the Q switch is set downwards (Q is false), current would flow, although this is forbidden by the truth-table for Implication. We must therefore prohibit the connection of both switches to singly connected points, whenever three wires are in use interconnecting the switch points.

This prohibition can be lifted provided we introduce a certain transformation of the diagrams with three lines. To do this, we can allow the use of the P and Q poles as connection points. The poles are those points in Figure 4 where there are arrows. By using them, as shown in Figure 12, we see it is possible to employ four different connections, each of which represents a "T" of "1" in two truth-table rows. Now, in the case of Implication, we can express the function as having a "1" in Rows 1 and 3, and in Rows 3 and 4. This double mention of Row 3 is, of course, quite innocuous. We can, therefore, transform the original "Z" diagram for Implication into a diagram having only two lines, namely, those shown for Rows 1, 3 and Rows 3, 4 in Figure 12. See Figure 13. No undesired completion of the circuit can then occur when P is set at 1 and Q at 0. Moreover, the diagram of the Negation of Implication remains unaffected: it will be just the one line numbered 2 in Figure 4. For the other three possible diagrams using three lines, a similar transformation is easily found, as in the bottom of Figure 13. This method of transformation, as well as the prohibition mentioned above, need be taken into account only when one is planning an actual circuit; an operation like that done in Figure 9 can proceed as shown, since the three-line diagram disappears in the end.

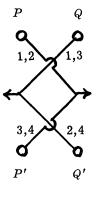
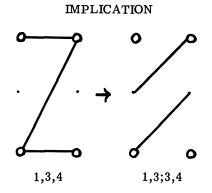


Figure 12



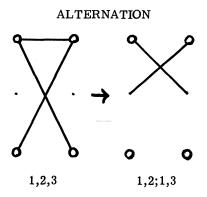


Figure 13