

Research Article

Dynamic Sliding Mode Evolution PWM Controller for a Novel High-Gain Interleaved DC-DC Converter in PV System

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Considering the disadvantages of the traditional high-gain DC-DC converter such as big size, high voltage stress of switches, and large input current ripple, a novel high-gain interleaved boost converter with coupled-inductor and switched-capacitor was proposed correspondingly and the operation principle together with the steady-state analysis of this converter was also described. Besides, a new control approach—dynamic sliding mode evolution PWM controller (DSME PWM) for the novel topological converter based on both dynamic evolution and sliding mode control was also presented. From the simulation results and experimental validation the proposed converter can fulfill high-gain boost, low ripple of both the input current and the output voltage. Furthermore, MPPT technique can be also achieved in a short time by simulation. The efficiency and stability of the converter proposed in this paper can be improved.

1. Introduction

Photovoltaic (PV) generation has an increasing influence on alleviating the energy crisis and reducing the environmental pollution. Researchers around the world have devoted themselves to the performance of PV system such as stability, efficiency, and the cost as a consequence (as discussed by [1–3]). Generally, the outputting voltage of the PV arrays ranges from 30 V to 60 V. High-gain and high-efficiency DC-DC converters are required to boost the low PV voltage to a high voltage, such as 380 V for the full-bridge inverter or 760 V for the half-bridge inverter in the 220 V AC grid-connected power system.

The good performances of any high-gain DC-DC converter in PV system greatly depend on the employed topology and the corresponding control strategy. So when designing this kind of converters, one should pay more attention to these two aspects and ensure that the designed converter can minimize the current ripple and reduce the numbers of the electrolytic capacitors, which can reduce the circuit cost and easily achieve MPPT algorithms (as discussed by [4, 5]). Besides, power losses that existed in the converters in high-output-voltage applications should be decreased to improve

system efficiency (as discussed by [6]). This paper will devote itself to a novel scheme that can meet the requirement above.

The traditional boost converters can achieve any high-gain transform by adjusting the duty cycle theoretically; however the actual voltage gain is often limited by the parasitic parameters of inductances, capacitances, and switch devices (as discussed by [7]). Furthermore, in high-gain applications, as the duty cycle increases, the input current ripple, voltage or current stress of the devices, and the switching loss are all increasing as well as the diodes' reverse recovery loss, decreasing the efficiency of the converters. Meanwhile electromagnetic interference (EMI) is further severe due to the excess of dv/dt . Boost converter can enhance its voltage gain via adding coupled inductances (as discussed by [8–10]). However, voltage spike will occur when turning off the switches due to the leakage inductances, which can result in voltage stress increasing, efficiency lowering, and severe EMI. The aforementioned problems can be relieved by active or passive clamping methods. Undoubtedly, it will make the main circuit, control strategy and drive mode more complicated (as discussed by [11, 12]). Another way to improve the voltage gain of conversion is to employ nonisolated cascade boost converters (as discussed by [13]).

However there are many disadvantages, such as low reliability, high costs, and complexity of main circuit as well as control strategy and drive methods; besides, the outputting diodes' reverse recovery problem is still serious in high-gain applications. Isolated boost converters can also achieve high-gain transform by designing the ratio of transformers (as discussed by [12, 14]), but the leakage inductances will cause many problems such as voltage overshoot of switches, big voltage stress, and EMI problems. Meanwhile the loss of transformers will result in lower efficiency, higher costs, and complexity of main circuit, control strategy, drive methods, and isolation design. The topology-combining boost converters and fly-back converters can be employed in the high-step-up transform (as discussed by [15, 16]), whose topology and control method are fairly simple; however the voltage balance of the capacitors exists in this system due to series connection.

The reverse-recovery loss of the output diode is one of the main reasons why the efficiency is limited in the high step-up applications. When the boost converter works on discontinuous current mode (DCM) or critical current mode (CRM), the reverse-recovery loss can be reduced, but it will increase both current stress and input current ripple. Therefore it is not suitable for the high-power applications due to the bulky filter circuit.

Interleaved boost converters can not only develop both power level and power density but also average the thermal stress distribution and reduce the input current ripple (as discussed by [17–19]), which can even be eliminated when the duty cycle is equal to 0.5 theoretically. However, there are some weaknesses to apply interleaved boost converter into PV grid-connected system directly (as discussed by [7, 18]). The step-up ratio is not increased efficiently comparing with the traditional single-stage boost converter, as well as the voltage stress of switches. Besides, it is very sensitive for ordinary interleaved boost converters to mismatch the duty cycle.

In allusion to all the problems mentioned above, a novel high-gain interleaved converter with coupled inductance and switched capacitor (hereinafter referred to as the new converter) is proposed. High-gain transform can be realized by designing the main circuit parameters reasonably. Furthermore, the topology as well as its control method is relatively simple. Compared with conventional interleaved boost converters, the new one can boost voltage on the great scale, while reducing the voltage stress of the switch devices significantly under the same duty cycle. Moreover, the volume of magnetic elements and the current ripple of the inductance can be reduced by introducing coupled inductance (as discussed by [8, 9, 14]).

Control strategy of the proposed converter can easily achieve the MPPT algorithms and minimize the current ripple to reduce the coupled inductance losses and to improve system efficiency and stability. Moreover, less computation should also be under the consideration to ease the computational complexity. It is worth noting that, in the literature, some examples of high-gain DC-DC converters are presented, but they only concern the topologies, while few papers are devoted to the controller design for such kind of converter, although not referring to PV applications.

Sliding mode control (SMC) has a high robustness against plant uncertainty and external disturbances, including those due to the environmental conditions in PV applications. Many SM-based MPPT algorithms operated in different applications or different topologies have been proposed in published papers, but most of those mainly focus on the SMC used in conventional boost converter. Nevertheless, such an approach has never been used in analyzing a class of interleaved boost converters for PV applications controlled by the SM-MPPT technique.

The controller of the proposed new converter is required to extract the maximum energy from the PV panels and output the stable expectant voltage without errors. Dynamic evolution control (DEC) as a new control technique has been utilized in power electronics converters (not in PV applications). DEC can ensure that the error state goes to zero in increase of time, thereby improving the dynamic characteristic of system.

A new control approach based on both SM-MPPT and DEC is proposed in this paper. Since the outputting voltage and current of PV cell together with the outputting voltage of converter are involved in calculation of duty cycle, all the variation above can be compensated in the dynamic evolution.

This paper is organized as follows. Section 2 describes the characteristic of PV cells. Section 3 gives the working principle and performance analysis of the new converter. Section 4 is devoted to the controller design on basis of SM-MPPT and DEC. Sections 5 and 6 afford the simulation results and experimental validation, respectively. In the conclusion, the main results are finally summarized.

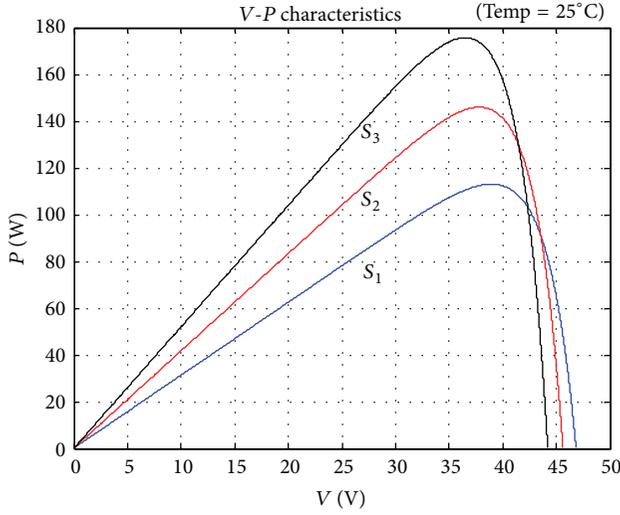
2. Characteristic of PV Cells

Formulas of the outputting current and power for the PV cells can be seen from (1) (as discussed by [3]) and Figure 1 shows the output characteristics of PV cells:

$$\begin{aligned} i_{pv} &= I_{ph} - I_{sat} \left[\exp \left(\frac{qV_{pv}}{AKT} \right) - 1 \right], \\ P_{pv} &= V_{pv}I_{ph} - V_{pv}I_{sat} \left[\exp \left(\frac{qV_{pv}}{AKT} \right) - 1 \right], \end{aligned} \quad (1)$$

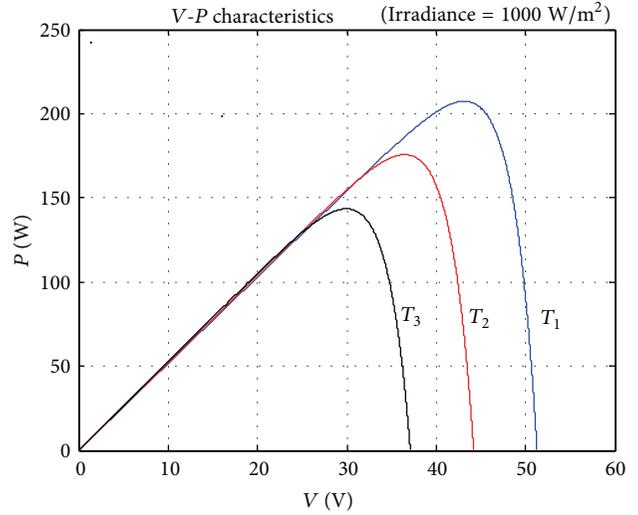
where i_{pv} , V_{pv} are the outputting current and voltage of PV cells, I_{ph} is the photocurrent of a single solar module, I_{sat} is the reverse saturation current, K is Boltzmann constant, q is electric charge, T is operating temperature, and A is P-N junction ideal factor.

When the output of the equivalent circuit of PV cells is shorted, if neglecting the reverse leakage current of the diodes, we can make an approximation that $I_{ph} \approx I_{sc}$ (I_{sc} is the short-cut current), which will be used in part V for analyzing the inputting current in dynamic mode.



- $S_1 = 600 \text{ (W/m}^2\text{)}$
- $S_2 = 800 \text{ (W/m}^2\text{)}$
- $S_3 = 1000 \text{ (W/m}^2\text{)}$

(a) V-P curve when temp. = 25°C, different irradiance



- $T_1 = 15^\circ\text{C}$
- $T_2 = 25^\circ\text{C}$
- $T_3 = 35^\circ\text{C}$

(b) V-P curve when irradiance = 1kW/m², different temp.

FIGURE 1: The output characteristics of PV cells.

3. Principle and Steady-State Analysis

3.1. Principle of the New Converter. The new converter with PV panels is shown in Figure 2. Capacitors C_1 , C_2 and diode VD_1 are employed to further enlarge the boost voltage under the same duty cycle compared with any other topology.

The inductances L_1 and L_2 are closely coupled and with the same winding orientation. The coupled inductances can be represented as a mutual inductance M , two equivalent leakage inductances L'_1 and L'_2 . The equivalent circuit is shown in Figure 3.

The relationships of the inductances are related by the following equations:

$$\begin{aligned} L'_1 &= L_1 - M, \\ L'_2 &= L_2 - M, \\ M &= k\sqrt{L_1L_2}, \end{aligned} \quad (2)$$

where k is coupled coefficient.

In order to simplify the circuit analysis of the proposed converter, several necessary assumptions should be made as follows.

- (1) All components including power switches, magnetic components, and diodes are ideal; the on-state resistance $R_{DS(ON)}$ and all parasitic capacitances of the switches are neglected, as are the forward voltage drops of diodes $VD_1 \sim VD_3$.
- (2) The ESR of capacitors $C_0 \sim C_2$ and the parasitic resistance of coupled inductances are neglected.
- (3) $L_1 = L_2 = L$.

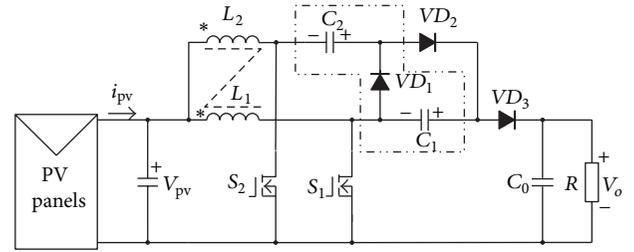


FIGURE 2: The new converter.

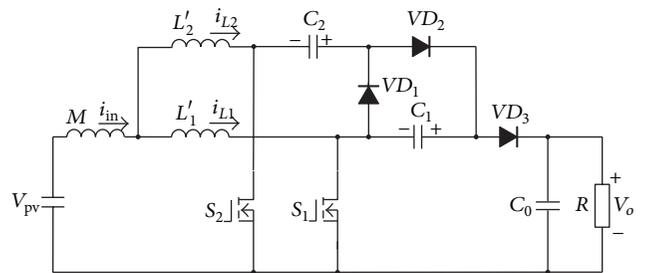


FIGURE 3: Equivalent circuit of the new converter.

- (4) S_1 and S_2 work by turn and both are driven by PWM signals.

Referring to the equivalent circuits for four different switching states of a switching period shown in Figure 4 and the waveforms in Figure 5, the operation of the converter can be explained as follows.

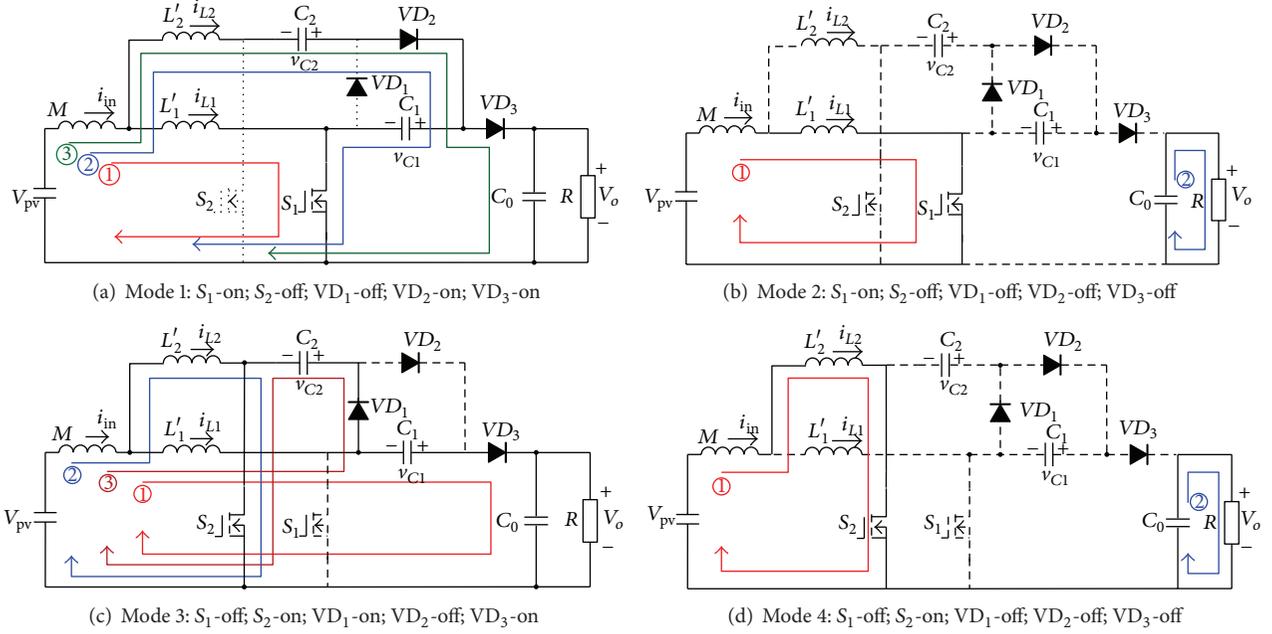


FIGURE 4: Operation states and current paths of the converter.

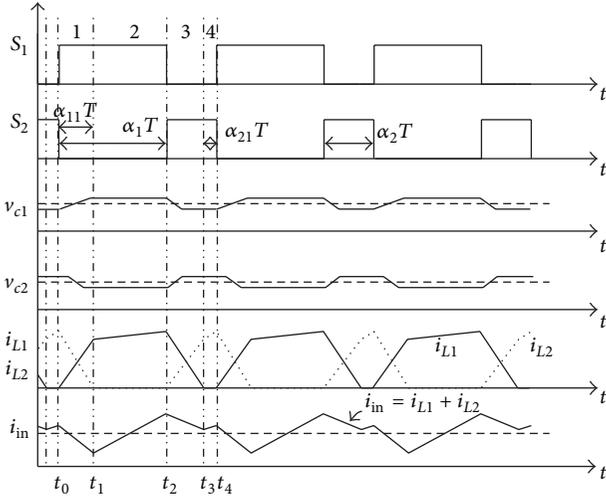


FIGURE 5: Main waveforms of the new converter.

Mode 1 (Figure 4(a)). At time t_0 , S_1 is on while S_2 is off; the current in the inductance L'_1 starts to rise linearly while L'_2 continues to discharge (the current in L'_2 was acquired in the last switching period). Capacitor C_2 discharges, leading to its voltage falling. But the voltage of capacitor C_1 rises because C_1 is charged; besides, capacitor C_0 is charged by input voltage and inductor in this mode. The rates of change of i_{L1} and i_{L2} are approximately given by

$$\begin{aligned} \frac{di_{L1}}{dt} &= \frac{V_o - v_{C1}}{L'_1}, \\ \frac{di_{L2}}{dt} &= -\frac{V_o - v_{C2}}{L'_2}. \end{aligned} \quad (3)$$

Mode 2 (Figure 4(b)). At time t_1 , i_{L2} falls to zero. i_{L1} continues to rise linearly. R is charged by capacitor C_0 . The rate of change of i_{L1} is

$$\frac{di_{L1}}{dt} = \frac{V_{pv}}{L_1}, \quad (4)$$

where $L_1 = L'_1 + M$.

Mode 3 (Figure 4(c)). At time t_2 , S_1 is off while S_2 is on. i_{L2} starts to rise linearly from zero and L_1 starts to discharge. Besides, C_1 discharges too while C_2 starts to charge. Moreover, C_0 is charged by input voltage and inductor. The rates of change of i_{L1} and i_{L2} are approximately given by

$$\frac{di_{L1}}{dt} = -\frac{V_o - v_{C1}}{L'_1}, \quad (5)$$

$$\frac{di_{L2}}{dt} = \frac{V_o - v_{C2}}{L'_2}, \quad (6)$$

$$v_{C1} + v_{C2} = V_o. \quad (7)$$

Mode 4 (Figure 4(d)). At time t_3 , S_1 is off while S_2 is on, i_{L1} falls to zero. i_{L2} continues to rise linearly. R is charged by capacitor C_0 . The rate of change of i_{L2} is

$$\frac{di_{L2}}{dt} = \frac{V_{pv}}{L_2}, \quad (8)$$

where $L_2 = L'_2 + M$.

The switching period will be repeated when S_1 is on again at time t_4 .

3.2. *Steady-State Analysis.* Assume that the current waveforms shown in Figure 5 have reached a steady state. From the waveform i_{L1} as shown in Figure 5, it can be found that

$$\frac{V_o - v_{C1}}{L'_1} \alpha_{11} T + \frac{V_{pv}}{L_1} (\alpha_1 - \alpha_{11}) T = \frac{V_o - v_{C1}}{L'_1} (\alpha_2 - \alpha_{21}) T. \quad (9)$$

From the waveform i_{L2} as shown in Figure 5, it can be found that:

$$\frac{V_o - v_{C2}}{L'_2} (\alpha_2 - \alpha_{21}) T + \frac{V_{pv}}{L_2} \alpha_{21} T = \frac{V_o - v_{C2}}{L'_2} \alpha_{11} T. \quad (10)$$

Also from Figure 5, the average values of i_{L1} and i_{L2} , denoted as I_1 and I_2 , respectively, are found as

$$\begin{aligned} I_1 &= \frac{1}{T} \left\{ \frac{1}{2} \frac{V_o - v_{C1}}{L'_1} \cdot (\alpha_{11} T)^2 + \frac{1}{2} \frac{V_o - v_{C1}}{L'_1} \cdot [(\alpha_2 - \alpha_{21}) T]^2 \right. \\ &\quad \left. + \frac{1}{2} (\alpha_1 - \alpha_{11}) T \cdot \left[\frac{2(V_o - v_{C1})}{L'_1} \cdot \alpha_{11} T + \frac{V_{pv}}{L_1} (\alpha_1 - \alpha_{11}) T \right] \right\}, \\ I_2 &= \frac{1}{T} \left\{ \frac{1}{2} \frac{V_o - v_{C2}}{L'_2} \cdot (\alpha_{11} T)^2 + \frac{1}{2} \frac{V_o - v_{C2}}{L'_2} \cdot [(\alpha_2 - \alpha_{21}) T]^2 \right. \\ &\quad \left. + \frac{1}{2} \alpha_{21} T \cdot \left[\frac{2(V_o - v_{C2})}{L'_2} \cdot (\alpha_2 - \alpha_{21}) T + \frac{V_{pv}}{L_2} \alpha_{21} T \right] \right\}. \quad (11) \end{aligned}$$

Assume that the converter is lossless; that is, the input power P_i is equal to the output power P_o . Consider

$$V_{pv} (I_1 + I_2) = \frac{V_o^2}{R}, \quad (12)$$

where R is the load resistance.

In principle, (7) and (9)–(12) can be solved to find V_o . However, to simplify the calculation, it is assumed that $\alpha_1 = \alpha$, $\alpha_2 = 1 - \alpha$, $L_1 = L_2 = L$, and $L'_1 = L'_2 = (1 - k)L$. According to some algebraic manipulations and solving a quadratic equation derived from (12), the approximate values of V_{C1} , V_{C2} , and V_o can be referred as follows:

$$V_{C1} = \frac{3}{1 - \alpha} V_{pv} = \frac{3}{4} V_o, \quad (13)$$

$$V_{C2} = \frac{1}{1 - \alpha} V_{pv} = \frac{1}{4} V_o,$$

$$V_o = \frac{4}{1 - \alpha} V_{pv}. \quad (14)$$

The effect of R on the calculation is very little; thus it is neglected when getting the approximate values, as shown in (13) and (14).

A careful study of the waveforms shown in Figure 5 will reveal the following interesting facts.

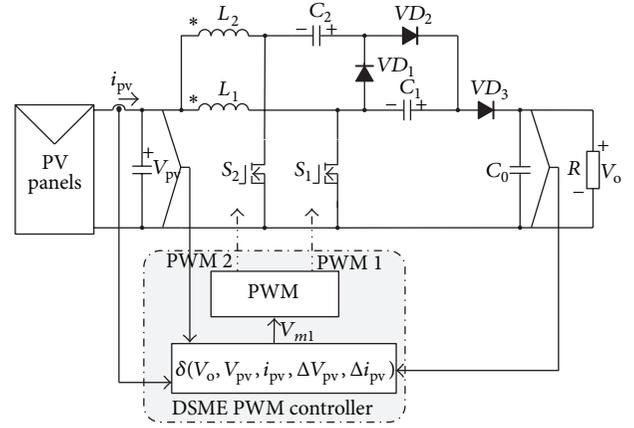


FIGURE 6: The control flow chart of DSME PWM controller.

- (1) As far as the input current i_{in} is concerned, the converter appears to operate in CCM (because i_{in} is continuous). Thus, the peak current stress of the inductances and the input current ripple can be maintained relatively low.
- (2) However, since i_{L1} and i_{L2} are discontinuous, the new converter is actually operating in DCM. Also, since the rectifier diodes $VD_1 \sim VD_3$ turn off before S_1/S_2 turns on, the reverse-recovery loss of the rectifiers is eliminated.
- (3) Besides, the current of inductance i_{L1}/i_{L2} has fallen to zero before S_1/S_2 turns on. ZCS soft switching operation during the whole switching transition is achieved.

Furthermore, when considering the parasitic resistances of switches and capacitances (r_s and r_c), the switching loss due to capacitances in the course of charging can be defined as (15) in an independent converter which contains n capacitances:

$$W_s = \frac{nC}{2} \cdot \frac{1 + e^{-\alpha T/\tau}}{1 - e^{-\alpha T/\tau}} (\Delta V_o)^2, \quad (15)$$

where C is the value of capacitances and $\tau = (r_s + r_c)C$.

From (15), W_s do exist even under the ideal conditions, mainly depending on ΔV_o . Thus, in order to reduce W_s , the difference between the maximum and the minimum of voltage in the course of charging for all capacitances should be decreased.

4. DSME PWM Controller

The original intention of the DSME control is to achieve MPPT as well as high-gain boost, also to reduce the error state by forcing the error state to follow the specific path, which ensures the error state goes to zero in increase of time (as discussed by [19, 20]). The control flow chart of dynamic sliding mode evolution PWM Controller can be seen in Figure 6.

The modulating signal of PWM generation V_{m1} is produced by the formula δ , combing the sliding mode theory

with the dynamic evolution algorithm. The specific design process of the DSME controller can be described as follows.

4.1. MPPT by Sliding Mode Control. When the PV cells run at the point of maximum power

$$\frac{dP_{pv}}{dV_{pv}} = i_{pv} + V_{pv} \frac{di_{pv}}{dV_{pv}} = 0. \quad (16)$$

In SMC, the state space is divided into $s > 0$ and $s < 0$ by sliding manifold ($s = 0$). The movement on $s = 0$ can be called sliding mode dynamics. Considering $dP_{pv}/dV_{pv} = 0$, the sliding manifold can be chosen as (as discussed by [21, 22])

$$s = \frac{dP_{pv}}{dV_{pv}} = i_{pv} + V_{pv} \frac{di_{pv}}{dV_{pv}}. \quad (17)$$

Reconsidering the mathematical model of PV cell,

$$i_{pv} = I_{ph} - I_{sat} \left[\exp\left(\frac{qV_{pv}}{AKT}\right) - 1 \right]. \quad (18)$$

Directly substituting i_{pv} from (18) into (17),

$$\begin{aligned} s &= \frac{dP_{pv}}{dV_{pv}} = i_{pv} + V_{pv} \frac{di_{pv}}{dV_{pv}} \\ &= -I_{sat} \left[\exp\left(\frac{q}{AKT} V_{pv}\right) \cdot \frac{q}{AKT} V_{pv} \right] \\ &\quad + I_{ph} - I_{sat} \left[\exp\left(\frac{q}{AKT} V_{pv}\right) - 1 \right] \\ &= -I_{sat} \left(\frac{q}{AKT} V_{pv} + 1 \right) \cdot \exp\left(\frac{q}{AKT} V_{pv}\right) + (I_{ph} + I_{sat}). \end{aligned} \quad (19)$$

The differential form of s is

$$\begin{aligned} \dot{s} &= -I_{sat} \frac{q}{AKT} \cdot \frac{dV_{pv}}{dt} \exp\left(\frac{q}{AKT}\right) - I_{sat} \left(\frac{qV_{pv}}{AKT} + 1 \right) \\ &\quad \cdot \exp\left(\frac{qV_{pv}}{AKT}\right) \frac{q}{AKT} \frac{dV_{pv}}{dt} \\ &= -I_{sat} \frac{q}{AKT} \cdot \frac{dV_{pv}}{dt} \exp\left(\frac{qV_{pv}}{AKT}\right) \left(\frac{qV_{pv}}{AKT} + 2 \right). \end{aligned} \quad (20)$$

According to $\dot{s} < 0$, if $s > 0$, then $\dot{s} < 0$, $dV_{pv}/dt > 0$, V_{pv} will increase when s tends to sliding manifold, and if $s < 0$, then $\dot{s} > 0$, $dV_{pv}/dt < 0$, V_{pv} will decrease when s tends to sliding manifold. The dynamic accommodation of V_{pv} can be seen in Figure 7.

Considering that the new converter is composed of two paralleled boost converters, the purpose of the additional switched capacitor and coupled inductance is to increase the voltage gain. Thus, the drive signals for the switches can be designed, respectively. From the state space model of the single boost converter, when the switch is on, V_{pv} increases

and when the switch is off, V_{pv} decreases (as discussed by [23]).

Rearranging (17),

$$s = \frac{dP_{pv}}{dV_{pv}} = i_{pv} + V_{pv} \frac{di_{pv}}{dV_{pv}} = V_{pv} \left(\frac{i_{pv}}{V_{pv}} + \frac{di_{pv}}{dV_{pv}} \right). \quad (21)$$

The differential form approximates to

$$\frac{\Delta i_{pv}}{\Delta V_{pv}} \approx \frac{di_{pv}}{dV_{pv}}. \quad (22)$$

Thus,

$$s = V_{pv} \left(\frac{i_{pv}}{V_{pv}} + \frac{\Delta i_{pv}}{\Delta V_{pv}} \right). \quad (23)$$

Theoretically, in the case of low requirement, both (17) and (24) can be chosen as the sliding surface:

$$s = \Delta V_{pv} \cdot i_{pv} + \Delta i_{pv} \cdot V_{pv}. \quad (24)$$

The corresponding control law is

$$u = \frac{1}{2} \left[1 + \text{sign}(\Delta V_{pv} \cdot i_{pv} + \Delta i_{pv} \cdot V_{pv}) \right]. \quad (25)$$

4.2. Evolution Path Selection. The principle of determining the evolution path is to ensure that the error state can go to zero at any increase of time (as discussed by [24, 25]). In this research, the evolution path is an exponential function as shown in Figure 8.

With this exponential evolution path, the value of the dynamic characteristic of the converter will decrease exponentially to zero by

$$H = H_0 e^{-\lambda t}, \quad (26)$$

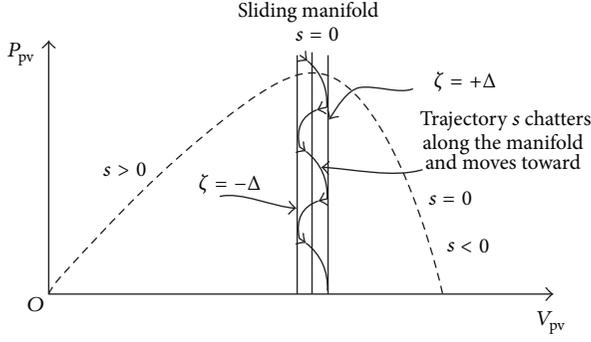
where H is the dynamic characteristic of system, H_0 is the initial value of H , and λ is a dynamic evolution factor. The derivative of H is

$$\begin{aligned} \frac{dH}{dt} &= -\lambda H_0 e^{-\lambda t} = -\lambda H, \\ \frac{dH}{dt} + \lambda H &= 0. \end{aligned} \quad (27)$$

4.3. Analysis of Duty Cycle. In order to synthesize the control law of the dynamic evolution controller, the dynamic equation of converter system has to be established and analyzed. On basis of the state space average model, when the converter works on DCM, the voltage and current dynamics of the converter are given by

$$V_{pv} = L \frac{di_{in}}{dt} + \frac{V_o}{4} (1 - \alpha), \quad (28)$$

where L is the inductance, V_{pv} is the input voltage, i_{in} is the input current, V_o is the output voltage, and α is the duty cycle, respectively.

FIGURE 7: The dynamic accommodation of V_{pv} .

$i_{in} \approx i_{pv}$, rearranging (28), the output voltage of converter can be written as

$$V_{pv} = L \frac{di_{pv}}{dt} + \frac{V_o}{4} (1 - \alpha), \quad (29)$$

$$V_o = 4V_{pv} + \alpha V_o - 4L \frac{di_{pv}}{dt}. \quad (30)$$

Define a linear voltage error function as shown below

$$E = ke_v = k(V_{ref} - V_o), \quad (31)$$

where $k > 0$.

Substituting (27) into (31), yields

$$k \frac{de_v}{dt} + \lambda ke_v = 0. \quad (32)$$

Combining (31) with (32)

$$k \frac{de_v}{dt} + (\lambda k - 1) e_v + V_{ref} = V_o. \quad (33)$$

Directly substituting the converter output voltage V_o from (30) into (33)

$$k \frac{de_v}{dt} + (\lambda k - 1) e_v + V_{ref} = 4V_{pv} + \alpha V_o - 4L \frac{di_{pv}}{dt}. \quad (34)$$

The obtained duty cycle formula is given by

$$\alpha = \frac{V_{ref} - 4V_{pv}}{V_o} + \frac{(\lambda k - 1) e_v}{V_o} + \frac{k}{V_o} \frac{de_v}{dt} + \frac{4L}{V_o} \frac{di_{pv}}{dt}. \quad (35)$$

Formula (35) forces the state error function E to satisfy the dynamic evolution function (27). Consequently, the state error function E is forced to make evolution by following equation (35) and decrease to zero ($E = 0$) with a decrease rate λ . The outputting voltage of converter converges to the converters steady state:

$$V_o = V_{ref}. \quad (36)$$

From the synthesis procedure, it is clear that the dynamic evolution controller works on the full nonlinear system and

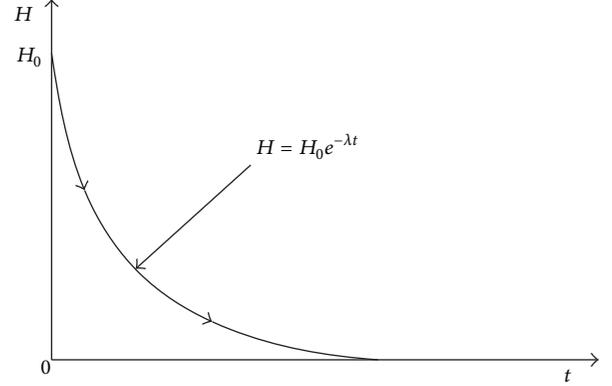


FIGURE 8: Exponential evolution path.

does not need any linearization or simplification on the system model at all and it is interesting to note that the control law in (35) consists of four distinct parts. The first part is the feed-forward term which is calculated based on the duty cycle at the previous sampling instant. This term compensates for variations in the input voltages. The second and third terms consist of proportional and derivative terms of the perturbations in the output voltage, respectively. The last term consists of the derivative terms of the inductance current. Since the inputting and outputting voltages and inductance current are involved in calculation of duty cycle, it can compensate all the variation of them in the dynamic evolution.

It should be noted that both V_{pv} and i_{pv} are not the voltage and current at the MPP in (35). Consequently, we expect that the controller can achieve MPPT and high-gain boost; thus considering the logic relationship of control signals, the final control law can be described as follows combing (25) with (35):

$$\delta = \frac{1}{2} \left[1 + \text{sign} \left(\Delta V_{pv} \cdot i_{pv} + \Delta i_{pv} \cdot V_{pv} \right) \right] \cdot \left(\frac{V_{ref} - 4V_{pv}}{V_o} + \frac{(\lambda k - 1) e_v}{V_o} + \frac{k}{V_o} \frac{de_v}{dt} + \frac{4L}{V_o} \frac{di_{pv}}{dt} \right). \quad (37)$$

4.4. PWM Generation. The PWM signals are generated by comparing a control signal with a constant peak repetitive triangle signal (V_{cs}). The frequency of the repetitive triangle signal establishes the constant switching frequency.

Figure 9 shows the PWM signals generation technique. PWM1 is produced when the control signal V_{m1} is greater than V_{cs} while PWM2 is produced when V_{m1} is less than V_{cs} .

The values of the desired duty cycle α can be gotten from (37). PWM signals are generated by (39):

$$V_{m1} = \delta, \quad (38)$$

$$\begin{aligned} \text{PWM1} &= \begin{cases} 1 & V_{m1} > V_{cs} \\ 0 & V_{m1} < V_{cs} \end{cases} \\ \text{PWM2} &= \begin{cases} 1 & V_{m1} < V_{cs} \\ 0 & V_{m1} > V_{cs} \end{cases} \end{aligned} \quad (39)$$

5. Simulation

Some simulation has been done in order to verify the performance of the topology and the main parameters can be referred to in Table I.

The portion of the simulation results is given in Figure 10.

Figure 10(a) shows the driving signals for S_1 and S_2 , which are generated by the control law δ . The outputting voltage and power of PV cell in process of MPPT can be seen in Figure 10(b). From the simulation, one may get the conclusion that the DSME PWM controller can ensure that the PV cell runs at the maximum power point in a short time. Although the overshoot with a little range occurs in the process of power adjustment, it will be eliminated soon and the stable outputting power of 260 W is achieved. During the dynamic adjustment, there is a stable and fleet performance without oscillation.

In Figure 10(c), the dynamic response of the novel topology is the curve labeled overall trend. This curve shows that the converter can raise the voltage from 36 V to 400 V steadily without a long time. The curve labeled partial enlargement shows that the outputting voltage has a low voltage ripple when it is in stable state. Considering the whole PV grid-connected system, a DC-link high voltage with low ripple is convenient to choice and maintaining of the DC-link capacitor.

As mentioned before, the converter can run under four modes in every switching period. The tendencies of i_{L1} and i_{L2} as well as i_{in} in every mode have been discussed in part III and it is also easy to get the conclusion about $i_{in} = i_{L1} + i_{L2}$ based on Kirchhoff's current law, so the tendency of i_{in} can be obtained by the sum of i_{L1} and i_{L2} . The first and second one of Figure 10(d) describe the stable current of i_{L1} and i_{L2} and i_{in} , respectively, over the same period in stable mode. Figure 10(d) shows that the current i_{in} has little ripple, which can reduce the coupled inductance losses and improve system efficiency.

Figure 10(e) shows the voltage waves of switched capacitors C_1 and C_2 . The voltage of C_1 is three times as much as the one of C_2 , close to three quarters of V_o ; this simulation verifies the formula (13).

6. Experiments

Experiments have been finished in our laboratory just in order to verify the validity of theoretical analysis above and the performance of the new converter proposed in this paper.

Experimental waveforms of the new converter are shown in Figure 11. The driving signals of S_1 and S_2 from DSP on basis of the algorithm in this paper are given in Figure 11(a). Obviously, the new converter can raise the voltage from 36 V to 400 V when the duty cycle equals 0.64 (calculated

TABLE 1: The main parameters.

Parameters	Values
V_{oc}/V	44.3
I_{sc}/A	7.7
V_{mp} at MPP/V	36
I_{mp} at MPP/A	7.2
Coupling coefficient	0.9
L_1 and L_2/mH	0.4
$C_1/\mu F$	10
$C_2/\mu F$	100
$C_0/\mu F$	22
$R/k\Omega$	1
Switching frequency/kHz	50

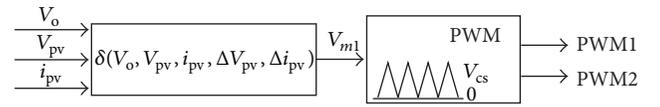


FIGURE 9: PWM generator.

from Figure 11(a)). The output voltage wave (after 10 times attenuation) is shown in Figure 11(b). Moreover, the ripple of the output voltage shown in Figure 11(b) can be limited in 8 V, which can decrease the loss of switched capacitors as shown in (15). Figure 11(c) shows the wave of the input current. The little input current ripple can reduce both the loss and the volume of the coupled inductance. Figures 11(d) and 11(e) show the voltage waveform of switched capacitors C_1 and C_2 , respectively (after 10 times attenuation). The voltage of C_1 , about 300 V~306 V, is three times as much as the one of C_2 , about 92 V~100 V, which is consistent with both the analysis and the simulation results above; besides, the difference between the maximum and the minimum of voltage in the course of charging for each capacitance can be limited to a fairly small range, which can decrease the loss of switched capacitors.

Burrs existing in experimental waveform mainly stem from the effect of EMI in the experiment.

7. Conclusion

This paper proposed a new high-gain interleaved converter with coupled inductances and switched capacitors network which are suited for PV application. After explaining its operating principle and analyzing its steady-state performance, then a control strategy for it on basis of SM-MPPT and DEC theory was designed. Both simulation analysis and experimental results showed that the proposed system had the following good performance.

- (1) Achieving MPPT and producing a high-gain voltage in an extremely short time.
- (2) Decreasing the ripple of the outputting voltage, as well as the inputting current and improving power density.

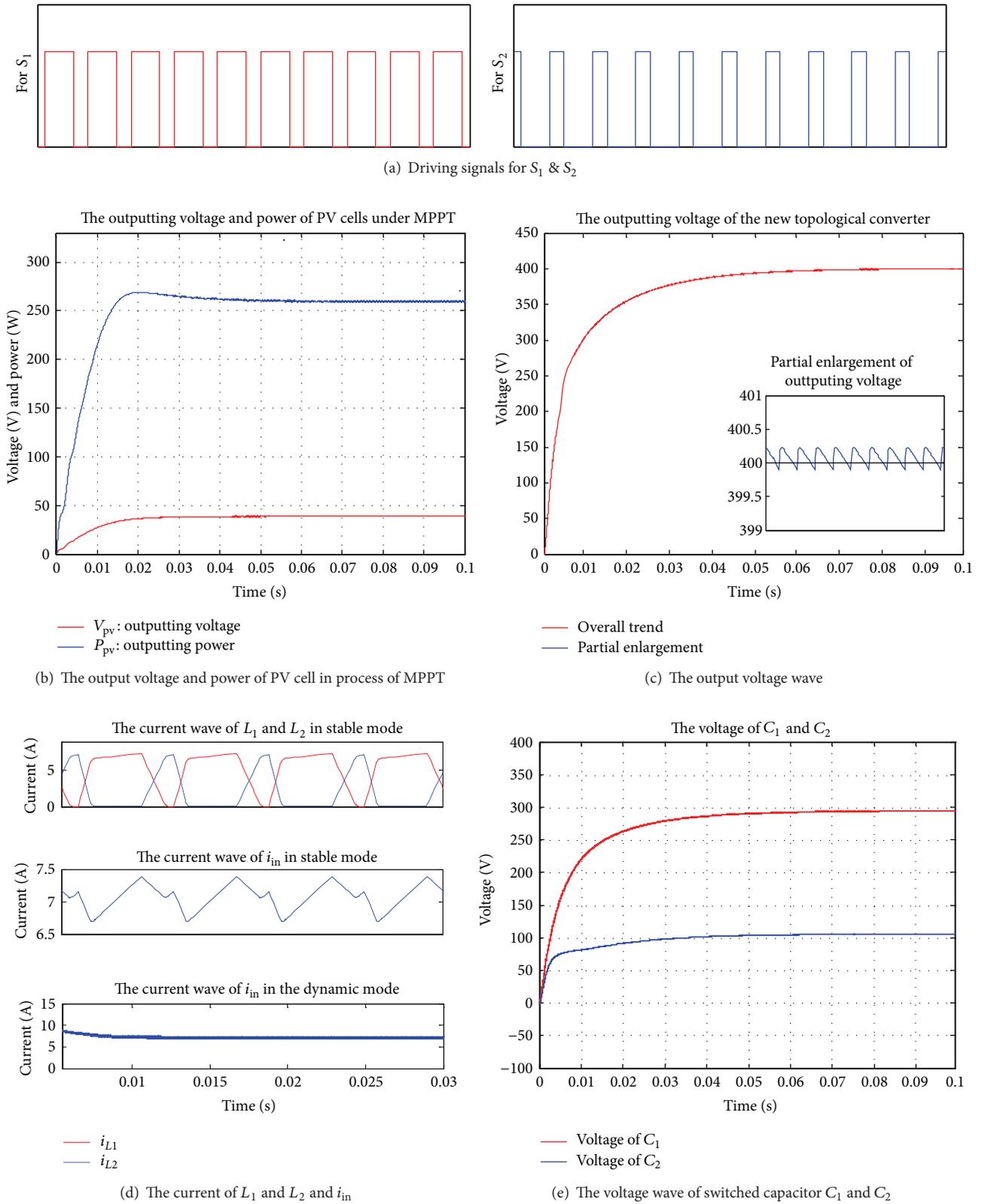


FIGURE 10: Simulation results.

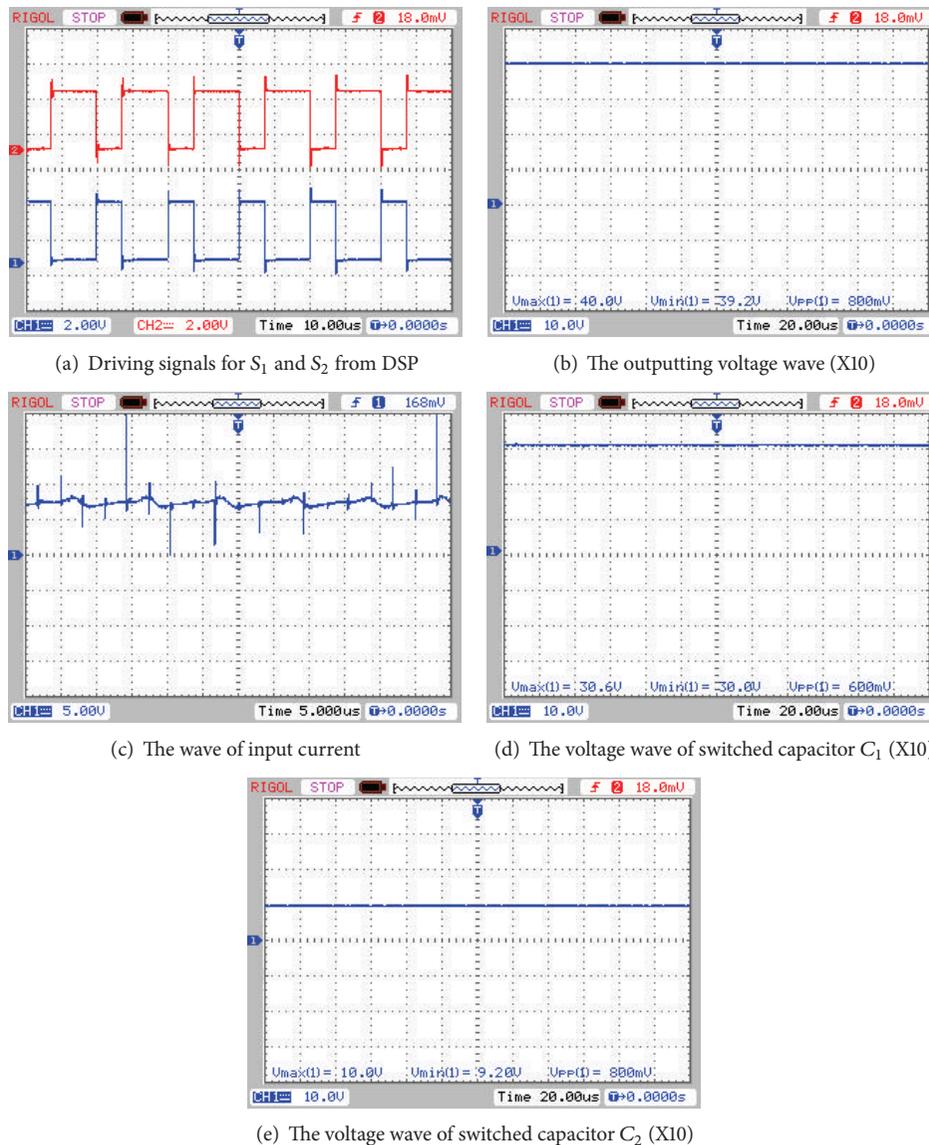


FIGURE 11: Experimental validation.

- (3) Reducing the volume of magnetic components and cutting the cost of system.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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